

# NP60N04MUK, NP60N04NUK

# MOS FIELD EFFECT TRANSISTOR

R07DS0597EJ0100 Rev.1.00 Jan 11, 2012

## **Description**

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

## **Features**

• Super low on-state resistance

 $R_{DS(on)} = 4.3 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 30 \text{ A})$ 

- Low  $C_{iss}$ :  $C_{iss} = 2450 \text{ pF TYP.} (V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

## **Ordering Information**

Part No.	Lead Plating	Packing	Package
NP60N04MUK-S18-AY *1	Pure Sn (Tin)	Tube 50 p/tube	TO-220 (MP-25K)
NP60N04NUK-S18-AY *1			TO-262 (MP-25SK)

Note: \*1 Pb-free (This product does not contain Pb in the external electrode)

# **Absolute Maximum Ratings** $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	40	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±60	А
Drain Current (pulse) *1	I <sub>D(pulse)</sub>	±240	А
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	105	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.8	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to 175	°C
Repetitive Avalanche Current *2	I <sub>AR</sub>	28	А
Repetitive Avalanche Energy *2	E <sub>AR</sub>	78	mJ

Notes: \*1  $\,T_{C}$  = 25°C,  $P_{W} \leq$  10  $\mu s,\, Duty\,\, Cycle \leq$  1%

## **Thermal Resistance**

Channel to Case Thermal Resistance  $R_{th(ch-C)}$  1.43 °C/W Channel to Ambient Thermal Resistance  $R_{th(ch-A)}$  83.3 °C/W

<sup>\*2</sup> R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V

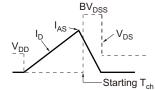
# **Electrical Characteristics** (T<sub>A</sub> = 25°C)

Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	1	μΑ	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
Forward Transfer Admittance *1	y <sub>fs</sub>	22	44	_	S	$V_{DS} = 5 \text{ V}, I_{D} = 30 \text{ A}$
Drain to Source On-state Resistance *1	R <sub>DS(on)</sub>	_	3.6	4.3	mΩ	$V_{GS} = 10 \text{ V}, I_{D} = 30 \text{ A}$
Input Capacitance	C <sub>iss</sub>	_	2450	3680	pF	V <sub>DS</sub> = 25 V
Output Capacitance	Coss	_	340	510	pF	$V_{GS} = 0 V$
Reverse Transfer Capacitance	C <sub>rss</sub>	_	140	260	pF	f = 1 MHz
Turn-on Delay Time	t <sub>d(on)</sub>	_	19	50	ns	$V_{DD} = 20 \text{ V}, I_D = 30 \text{ A}$
Rise Time	t <sub>r</sub>	_	9	30	ns	V <sub>GS</sub> = 10 V
Turn-off Delay Time	t <sub>d(off)</sub>	_	45	90	ns	$R_G = 0 \Omega$
Fall Time	t <sub>f</sub>	_	7	20	ns	
Total Gate Charge	$Q_{G}$	_	42	63	nC	V <sub>DD</sub> = 32 V
Gate to Source Charge	$Q_{GS}$	_	11	_	nC	V <sub>GS</sub> = 10 V
Gate to Drain Charge	$Q_{GD}$	_	11	_	nC	$I_D = 60 \text{ A}$
Body Diode Forward Voltage *1	$V_{F(S-D)}$	_	0.9	1.5	V	I <sub>F</sub> = 60 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>	_	44	_	ns	I <sub>F</sub> = 60 A, V <sub>GS</sub> = 0 V
Reverse Recovery Charge	Q <sub>rr</sub>	_	40	_	nC	di/dt = 100 A/μs

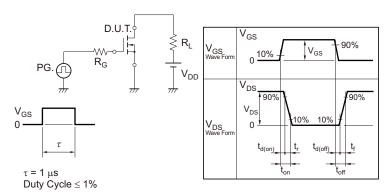
Note: \*1 Pulsed test

## **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $V_{GS} = 20 \rightarrow 0 \text{ V}$ $V_{GS} = 20 \rightarrow 0 \text{ V}$



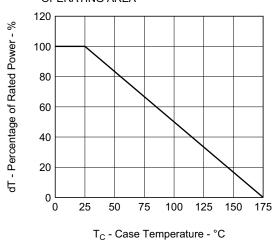
## **TEST CIRCUIT 2 SWITCHING TIME**



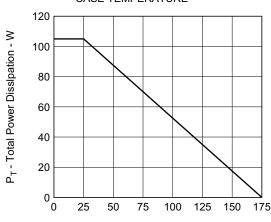
# **TEST CIRCUIT 3 GATE CHARGE**

# **Typical Characteristics** $(T_A = 25^{\circ}C)$

# DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

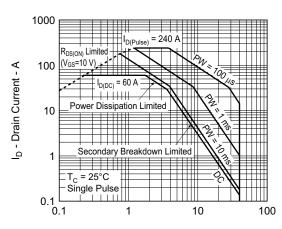


# TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



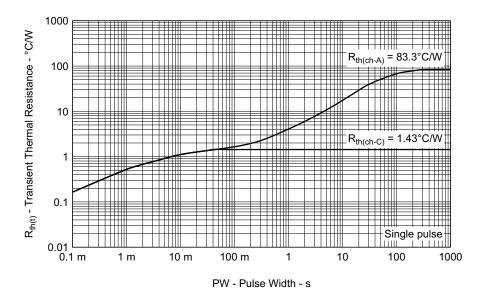
T<sub>C</sub> - Case Temperature - °C

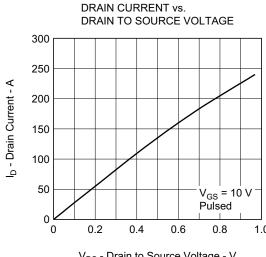
## FORWARD BIAS SAFE OPERATING AREA

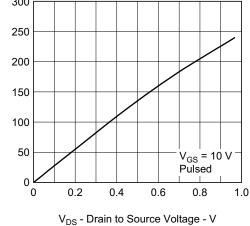


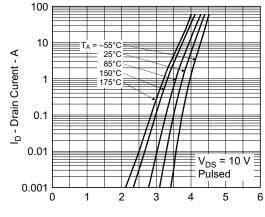
 $V_{DS}$  - Drain to Source Voltage - V

#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH





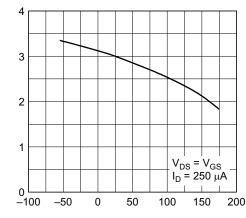




FORWARD TRANSFER CHARACTERISTICS

V<sub>GS</sub> - Gate to Source Voltage - V

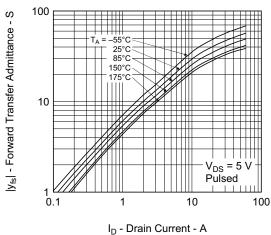




V<sub>GS(th)</sub> - Gate to Source Threshold Voltage - V

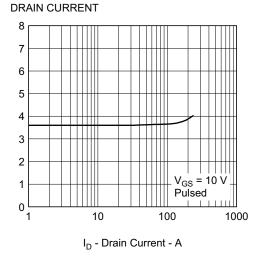
 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 



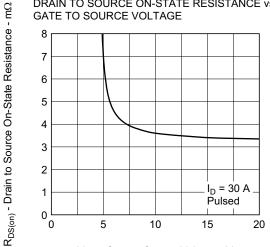


# DRAIN TO SOURCE ON-STATE RESISTANCE vs.

T<sub>ch</sub> - Channel Temperature - °C



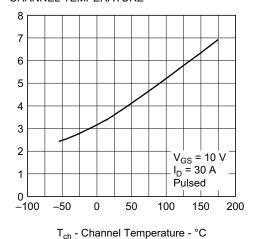
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



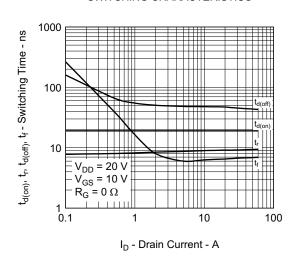
V<sub>GS</sub> - Gate to Source Voltage - V

 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 

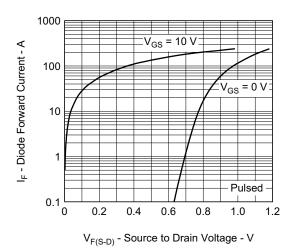
#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



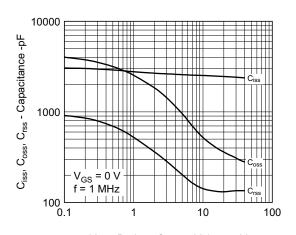
## SWITCHING CHARACTERISTICS



## SOURCE TO DRAIN DIODE FORWARD VOLTAGE

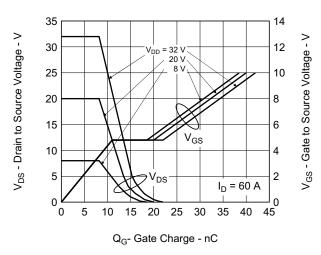


#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

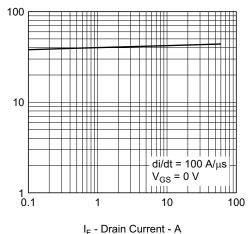


V<sub>DS</sub> - Drain to Source Voltage - V

#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS



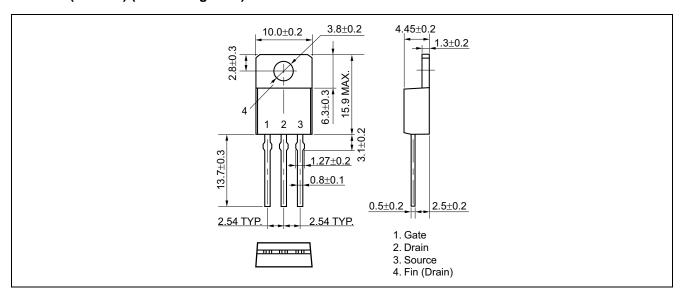
REVERSE RECOVERY TIME vs. **DRAIN CURRENT** 



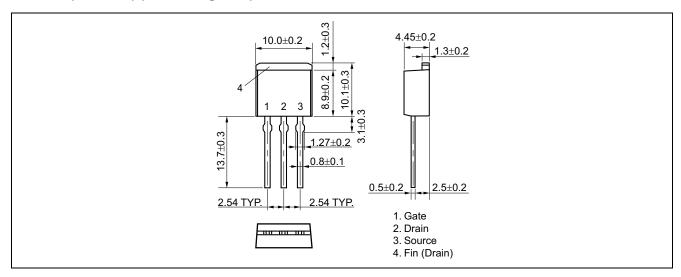
t<sub>rr</sub> - Reverse Recovery Time - ns

# Package Drawing (Unit: mm)

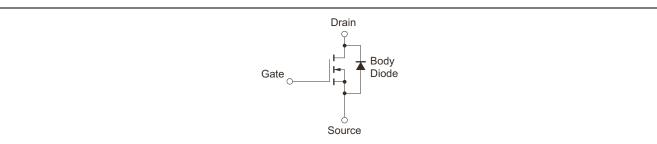
## TO-220 (MP-25K) (Mass: 1.9 g TYP.)



## TO-262 (MP-25SK) (Mass: 1.8 g TYP.)



# **Equivalent Circuit**



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

**Revision History** 

# NP60N04MUK, NP60N04NUK Data Sheet

		Description				
Rev.	Date	Page	Page Summary			
1.00	Jan 11, 2012	_	First Edition Issued			

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